Cover Letter to Commissioner for Patents

Please find attachments listed below:

1. Drawings amendment file "dspmsp_resp1-draw_08sep09.pdf";
2. Specification amendment file "dspmsp_resp1-spec_08sep09.pdf";
3. Claims amendment file "dspmsp_resp1-clm_08sep09.pdf";
4. Extension Request form ""dspmsp_resp1-extreq_08sep09.pdf";

Applicant's detailed responses to the Office Action are provided below.

Ad. 2

Such IDS is supplied herein as 3. Citations List (see "dspmsp_resp1-spec_08sep09.pdf") which shall be inserted at the end of BACKGROUND OF THE INVENTION as the 3rd subsection.

Foreign publications (Cit. 3, 2 and 9) are delivered in the next eBusiness session to avoid overload by long pdf files..

Ad. 3

The broader figure illustrating major system components and their interfaces is attached herein as the New Sheet comprising FIG.1A (see "dspmsp_resp1-draw_08sep09.pdf") which shall be inserted before all the other drawings listed as FIG.1 - FIG.4B.

Ad. 4

BRIEF DESCRIPTION OF THE DRAWINGS has been attached herein (see "dspmsp_resp1-spec_08sep09.pdf") and shall be inserted after SUMMARY OF THE INVENTION and before DESCRIPTION OF THE PREFERRED EMBODIMENTS.

Ad 5 and 6

Claims 70 and 83 are canceled

Ad. 7 and 8

Since the New Sheet supplies FIG.1A, which shows major system components and their interfaces without introducing any new subject matter, such rejection shall be withdrawn.

However such rejection indicates that basic facts related to the original drawings and specification need to be clarified.

All interconnect signals between the original drawings FIG.1 to FIG.4B have unique names identifying their sources and destinations explained comprehensively in the Description of the Preferred Embodiments utilizing the same names,

and inputs supplied from different drawings are connected at the top or left side and outputs are generated on the bottom due to the top-down or left-right data flow observed generally.

Therefore the office statement

"...the specification, including the figures, fails to adequately disclose how each sub-circuit is coupled to one another and how each sub-circuit interfaces with greater system as a whole"

is incorrect.

Similarly the follow-up statement

"While one of ordinary skill in the art would be able to assemble each sub-system individually, disclosure on how to assemble the greater system as a whole without undue experimentation is lacking"
is incorrect as well, since entire connectivity can be identified by reading of Description of the Preferred Embodiments defining it clearly.

Ad 9, 10 and 11
Claim 69 is amended.
Claim 87 is canceled.

Ad. 12

The data recovery solution presented in the teachings in US 6,987,817 (further named as DRS) is not covered by this patent claims which are limited clearly to the function of "measuring widths of a symbol in said input signal" and "adjusting said measured width in response to a correction signal".
Consequently such teachings of data recovery solutions shall be verified if they are enabling, since examination and granting of such claims, which do not cover DRS, obviously did not cover nor confirm such enabling abilities of DRS either.

As it is shown further below the sequential data recovery presented in this application (SDR) enables:

- **>10x more accurate and >10x faster phase/frequency detection & processing enabling SDR applicability to >10x faster links than the links which the DSR can be applied to;**
- **elimination of major stability and high error rate problems inherent for DSR.**

It shall be noticed that a phase jitter is the major factor limiting data rates (or link lengths) on high speed links while its impact is negligible on slow links (where lower data rates increase time interval unit (TIU) which the phase jitter is measured against).
Therefore conventional Analog CDR (ACDR) systems (working reliably at much lower cost & complexity & power-consumption) provide conclusively superior alternative to such digital DRS for the slow links, as ACDR jitter tolerance is fully sufficient for such lower data rates.
Consequently such DRS (much less efficient and less reliable as it is explained further below) can not enable any useful application for such lower data rates.
On the other hand such DRS (>10x slower than SDR) can not function on such high rate data links where insufficiency of ACDR jitter tolerance becomes such major limiting factor justifying search for such more complex digital solutions.
Therefore such DRS can not be considered to be an enabling solution and even more so if its inherent problems with stability and high error rates are taken into consideration (as they are explained further below).

Fundamental differences between the SDR and the DRS, are presented below.

A1. The way is substantially different as it is explained below.

SDR derives number of data bits received in an inter-transition interval, by performing:

- counting a number of entire sampling clock periods occurring during the inter-transition interval;
- deriving an integer estimate (equal to 0, 1 or 2) of a sum of a front phase delay between a front of the inter-transition interval and the first sampling clock edge, and an end delay between the last sampling clock edge and an end of inter-transitional interval;
- simple addition of such integer estimate to such periods number.

However DRS derives such data bits number by performing >10x more complex and >10x slower operations including:

- counting a number of entire sampling clock periods occurring during the inter-transition interval,
- multiplying such number by 16 (the number of oversampling sub-clocks);
- adding such multiplication result to such sum of front phase delay and end phase delay, in order to derive a lengths of the inter-transition interval expressed in the subclocks delays;
- dividing such lengths by an expected widths of data bit expressed in sub-clock delays.

B1. Consequently the results are substantially different as well:

- SDR enables data recovery from >10x faster transmission links than those accommodated by DSR, due to such >10x faster recovery of data bits from oversampled signal intervals;
- SDR enables > 10x lower power consumption than DSR , due to such >10x less intense processing.

A2 Furthermore the way is substantially different for still other reason explained below.

SDR utilizes maintaining a known frequency relation between the sampling clock and recovered data clock (accuracy <40ppm is very easy), for enabling such very simple use of sampling clock for the derivation of data bits number in the received interval.

On the other hand DRS utilizes such bit width (calculated by statistical processing of received intervals lengths), instead of sampling clock periods, for such complex derivation of bits number from the interval lengths measured in sub-clocks number.

B2 Consequently still other results are substantially different as well.

Such SDR utilization of frequency aligned sampling clock (instead of statistical bit width) for measuring intervals lengths, enables fundamental advantages listed below:

- much better accuracy of such aligned sampling clock in representing received data clock than that offered by the bit widths calculated statistically from the input signal subjected to an unknown random phase noise.
- elimination of accumulated division error caused by digitization error of bit width

during a long division of interval length by the bit width;

Consequently such SDR, securing much greater accuracy in lengths measurements and resulting much lower error rates, avoids serious problems with high error rates inherent for DRS.

Furthermore:
Since SDR uses such sampling clock instead of statistical bit widths, it avoids major stability problem and slow acquisition problem inherent for DRS as they are explained below.

- Since DRS's statistical processing is applied in a closed control loop (where such bit width provides feedback to the calculations of received interval length), it can make such close loop system inherently unstable by introducing unpredictable poles caused by the statistical processing responding to unknown phase noise in the received signal;
- Since DRS's statistical processing is very complex and very slow, it shall cause >100x longer acquisition times than those achievable with SDR.

Since the way and the result of such SDR are so substantially different in multiple major aspects, the DSR can not represent prior art to such SDR.

Furthermore:
Since such DRS is not enabling and such major novel contributions made by SDR are required to achieve such enabling capability, such DRS can not be useful for supporting any obviousness argumentation.

Since such substantially different (and highly superior) results have been achieved in the substantially different ways (involving intermediate inventions solving intermediate bottlenecks), such SDR shall be patentable.

Since recognition of differences between solutions requires learning new subjects, it is much more difficult than seeing similarities which relies on a knowledge possessed already.
Nevertheless these are the differences over previous art not similarities which need be considered in order to evaluate a novelty factor in compliance with the examination rules.
In order to facilitate such substantial examination work required by the advanced topics prosecuted herein; this response splits the application even further by limiting range of amended set of claims to much narrower subject matter.

The remaining parts of such fundamental DSP-MSP application will be filed later as divisional applications.

Ad 13
It is explained above in Ad 12 that the DRS (from US 6,987,817) is not an enabling solution and the way and the result of SDR are substantially different in multiple major aspects.
Therefore in view of such explanations, DRS can not anticipate SDR solutions prosecuted herein.

Ad 14
Such OR terminology should be acceptable in claims 68 and 69.
Claims 72 - 74, 76-78, and 80 are canceled.

Ad 15
In view of the explanations provided in Ad 12, DRS can not anticipate SDR solutions prosecuted herein.

Furthermore even if DRS were enabling, it's way and result are still fundamentally different than those of SDR.
It seems that similarity of elements taken out of context can not be useful for deciding novelty, as it can not be used as a right replacement of a comparison process based on researching differences between entire solutions such as DRS and SDR.
For example:
Since such statistical calculation of the bit widths is so essential for every DRS operation, it needs to be included in every set of DRS features brought up for comparing DRS with SDR.

Ad 16
In view of the explanations provided in Ad 12, DRS can not anticipate SDR solutions prosecuted herein.
Furthermore:
The SDR comprises a unique configuration of parallel processing phases, multiplying SDR processing throughput, which does not occur in US 6,987,817.
It seems that such substantial difference having significant impact on performance, can not be over-written by certain similarity between sequentially connected circuits of DRS and sequential processing stages of SDR.

Ad 17 - 26
All the claims mentioned in there are canceled.

Conclusion

Based on the application amendments and the above clarifications, it is thus respectfully submitted that the invention taught and defined herein by the claims embodies patentable subject matter.

The Examiner is earnestly solicited to give favorable consideration to this application and pass it to allowance.

Respectfully submitted,

By: John W. Bogdan on 09 / September / 2008